IMPLEMENTATION OF HARDWAREAPPROACH TO OFDM – MDC PIPELINE FFT PROCESSOR

A project report submitted in the partial fulfillment of the requirements for the award of degree of

BACHELOR OF TECHNOLOGY

IN

ELECTRONICS & COMMUNICATION ENGINEERING

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CERTIFICATE

This is to certify that the project work entitled **"IMPLEMENTATION OF HARDWAREAPPROACH TO OFDM – MDC PIPELINE FFT PROCESSOR"** is being submitted for the partial fulfillment of requirements for the award of Bachelor of Technology of in Electronics & Communication Engineering is a bona-fide work done by **S.UMA(21815A0419), R.DHUSYANTH(20811A0460), S.RAJESH (20811A0464), V.POOJITHA (20811A0474)** under guidance during year 2023– 2024 and it has been found suitable for acceptance according to the requirements of the University.

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ABSTRACT

The FFT/IFFT processor is widely used in various areas such as 4G telecommunications, speech and image processing, medical electronics and seismic processing, etc. In this paper an efficient implementation of FFT/IFFT processor for Multiple input Multiple output- orthogonal frequency division multiplexing (MIMO-OFDM) systems with variable length is presented. This paper opts memory scheduling and Multipath Delay Commutator (MDC) as the hardware architecture. Radix-Ns butterflies are used at each stage, where Ns denote the number of data streams, so that there is only one butterfly is used in each stage. For area and time optimization and to reduce power consumption, the Read Only Memories (ROM'S) which is used to store twiddle factor is replaced by complex multiplier. The design reduces the use of logic elements & 100% utilization rate is achieved. The result shows the advantages of the proposed scheme in terms of area and power consumption.

Keywords: Fast Fourier transform (FFT), Memory scheduling, Complex multiplier, Multiple Input Multiple Output(MIMO), OFDM.